7 Current Testing

7.1 Introduction

Functional testing detects faults on the logic level. The logic values are determined by measuring the voltage on the primary outputs. Voltage testing is effective in detecting stuck-at faults, particularly in bipolar technology. However, this type of testing does not guarantee detection of other faults beyond stuck-at faults in CMOS technology, which is the most popular technology at present. Another issue with voltage testing is the complexity of test pattern generation for large circuits. As we will see in this chapter, test sets for current testing are typically shorter than stuck-at fault tests. In addition, current testing is also effective in detecting stuck-at faults.

The concepts of fully complementary MOS (CMOS) have been known since the early 1960s [Wanlass 1961]. The interest in this technology was mainly because of its low power characteristics. The circuit draws current only during switching. Under static conditions, the quiescent current is due to leakage and it is too small to cause any thermal problems. The first device produced consumed just a few nanowatts of standby power [Riezeman 1991]. RCA announced the successful fabrication of a CMOS IC in 1968, and the first CMOS microprocessor was announced in 1974 [Noyce 1991]. From the onset, testing of CMOS circuits included monitoring of the quiescent current as part of parametric testing. Strong correlation has been found between this parametric testing and functional testing [Daniels 1990]. Delays in the circuit [Nelson 1975] have resulted in promoting current testing called I_{DDQ} testing. This is the current drawn from the power supply, V_{dd}, and Q stands for quiescent. This current was shown to be elevated for various CMOS defects, including bridging faults and SAF [Levi 1981, Malaiya 1982]. However, only in the late 1980s did current testing became very popular [Hawkins 1985] and has been integrated in CAD tools [Fritzemeier 1991]. At present, it is also used in conjunction with DFT constructs such as scan-path and Built-in Self-test (BIST), and memory testing [Soden 1992].

I_{DDQ} testing relies on the fact that CMOS devices have very low leakage current when the network is in the quiescent state. By monitoring this current, any manufacturing process that causes excessive leakage current is detected. To detect the higher currents due to a defect with an I_{DDQ} test, it is important that the defective network's quiescent current be significantly higher than that of the good network. This should take into account the variation in quiescent current for the good network due to process variation and the inaccuracies in measuring the quiescent current. In Fig. 7.1 the first normal distribution depicts the quiescent current of the good product with a mean value

Copyright © 2000 by John Wiley & Sons

denoted by Mg. The defective parts, which may draw excessive current, have their own distribution, with higher values for the quiescent current (mean Md) If the two distributions are far apart, a quiescent current limit can be selected that demarcates the good product from the defective product.

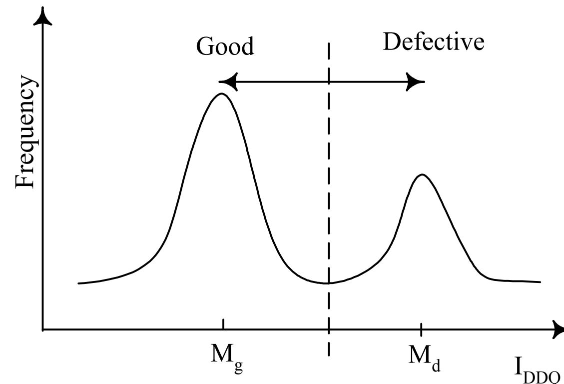


Figure 7.1 A General Distribution of IDDQ Values in CMOS Circuits

Current testing is not, however, a panacea. It has its problems. To measure the current adequately is possible only by using appropriate instrumentation. In addition, for deep-sub-micron (DSM) technology, the quiescent current becomes too high to be differentiated due to an increase in the subthreshold component [Williams 1996, Righter 1996].

7.2 Basic Concept

An IC consists of several million transistors forming different logic gates. Any of these gates can be, without loss of generality, modeled by an inverter. Let us consider a CMOS inverter and observe the switching currents for fault-free and faulty conditions. As the input voltage switches from 0 to V_{dd}, the PMOS, which is initially on, turns off and the NMOS transistor, which is initially off, turns on. During the switching time, t_f, the gate voltage is at values that cause both transistors to be on simultaneously. It is during this and only this period that a current flows between the power and ground rails as approximated in Fig. 7.2. Here we assume that when the transistors are not switching, the quiescent current of the circuit is negligible. In subsequent sections, we take a closer look at the actual value of this current.

Copyright © 2000 by John Wiley & Sons

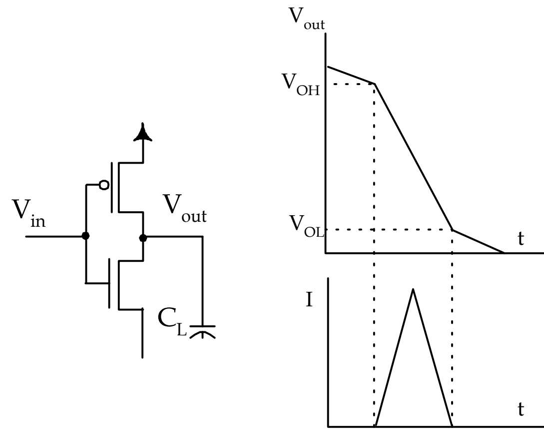


Figure 7.2 Switching Current in an Inverter

A more realistic waveform for the switching voltage and current in a CMOS inverter with minimal dimension in 1.2-μm technology is shown in Fig. 7.3. This is the result of PSPICE simulation. The upper curve is the input waveform. It is followed by the corresponding current in a fault-free inverter. If the NMOS transistor is stuck on and the input voltage is high, the output is pulled down to ground through the *n*-channel. This condition masks the fault on the pull-down transistor. However, when Vgs = 0 (V2 in Fig. 7.3), the PMOS transistor is on and the current will flow steadily between V_{dd} and GND since the NMOS is stuck-on. As shown in Fig. 7.3, this current is noticeably larger than the switching current of the healthy inverter. Notice that it was sufficient to provoke the fault to make it observable. The test required to detect the fault is therefore independent of the position of the gate in the circuit. Current testing does not require propagating the fault to a primary output.

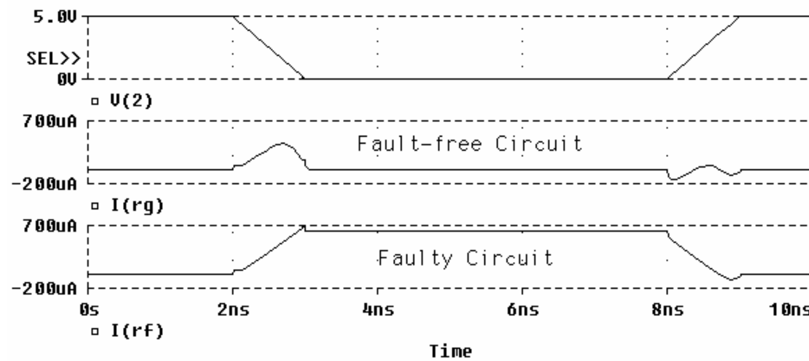


Figure 7.3 Spice Simulation for Fault free and Faulty Inverter

Normally, a circuit will consist of more than one gate switching in response to the pattern applied. The switching may be simultaneous or in succession. For example, in the NAND tree shown in Fig. 7.4, all inputs are kept high except for *S*, which is changed from low to high. Consequently, the output of all gates in the circuit will

Copyright © 2000 by John Wiley & Sons

switch. The switching currents for all gates of the tree are shown in Fig. 7.5. For the first NAND gate, the switching started at T1 = 5 ns and the last gate in the tree ended switching at T2 = 7.3 ns. Therefore, it is not accurate to measure the current for faulty behavior before time T*2*. That is, it is important to wait until the slowest gate switches before measuring the current. The duty cycle of the signal is to be long enough to ensure the switching of all gates. Thus it is critical to assess the fault-free current and the time taken for the circuit to settle down.

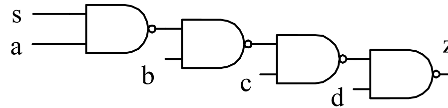


Figure 7.4 A NAND Tree

7.3 Fault-Free Current

7.3.1 Switching and Quiescent Currents

The switching current in a CMOS inverter is governed by

$$I = 0.5\beta_k[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] \tag{7.1}$$

where, $$\beta_k = \frac{\mu_k \varepsilon}{t_{ox}}(\frac{W_k}{L_k}) \tag{7.2}$$

As V_{gs} switches from low to high, or vice versa, the current passes through a peak that is the maximum of the expression in Eq. (1) as $V_{ds} = V_{gs} - V_t$:

$$I_{max} = 0.5\beta_k[(V_{gs} - V_t)^2 \tag{7.3}$$

where . is the device conductance, ε the permittivity, t_{ox} the gate oxide thickness, $_k$ the electron mobility, and W_k and L_k are the channel width and length of the transistor. The index *k* stands for the *n*-channel and *p*-channel, respectively. The current is at its maximum as $V_{ds} = V_{gs} - V_t$. At such an instant, there is a direct path between the power and ground rails. As we realized in Section 7.2, this current is much higher than the quiescent current.

Copyright © 2000 by John Wiley & Sons

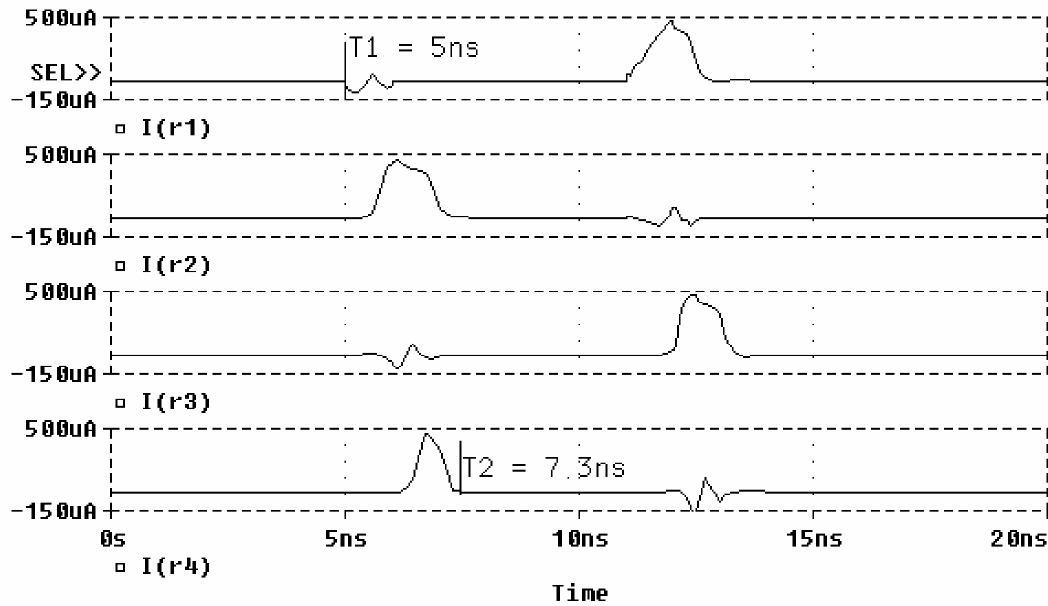


Figure 7.5 Switching Current in the NAND Tree

When the transistors are not switching, one of them will be in the on state, $V_{gs} > V_t$, and the others are in the off state, $V_{gs} = 0$. In the off state, the transistor is still conducting. This is known as *subthreshold* or *weak inversion conduction*. The change of subthreshold current with V_{gs} is shown in Fig. 7.6, which indicates the exponential characteristic of this region. The actual quiescent current is the sum of all off-state transistor currents. Measurements of this current for representative ICs are listed as a function of the number of transistors in Table 7.1 [Soden 1996]. A mean value of the current is given since different chips of the same size will yield a distribution around the mean.

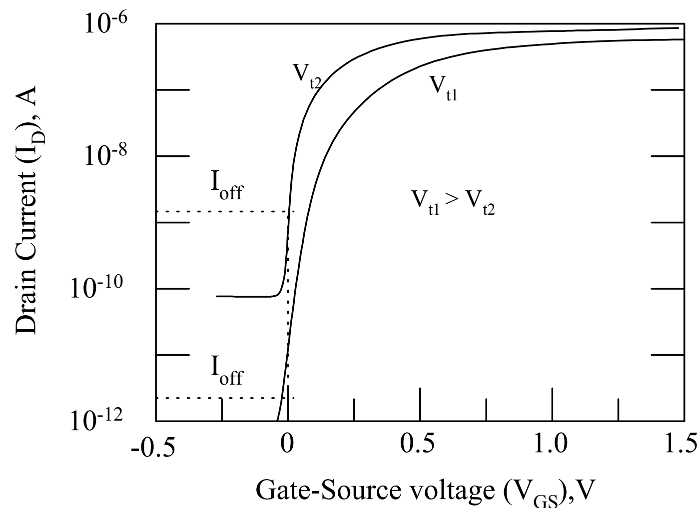


Figure 7.6 Sub-threshold Current or the (Off-State Current)

Copyright © 2000 by John Wiley & Sons

As a MOSFET's dimensions enter the submicron region, the subthreshold current increases due to scaled-down threshold voltages and short-channel effects, such as *drain-induced barrier lowering* (DIBL) and *punch-through* [Soden 1996]. These phenomena, as well as the increase in the number of transistors integrated in a single chip, cause the defect-free I_{DDQ} current to be elevated, as we describe in Section 7.7.

Table 7.1 Typical Values for I_{DDQ}

Transistor count in thousands	Mean I_{DDQ} (nA)
70	0.4
1500	320
6000	980

7.3.2 Switching Delays

The duration of current flow depends on the parameters of the transistors and the load on the output. The relation between the current, its duration, and voltage across the load capacitance is governed by

$$\int_{V1}^{V2} C dv = \int_{0}^{\tau} i dt$$

where τ is the time taken for the voltage to switch from V_1 to V_2. The values of V_1 and V_2 depend on whether the gate is switching from low to high, or vice versa. In the first case the load capacitance is charging through the *p*-channel and in the second case it is discharging through the *n*-channel. Also, depending on the values of *V*1 and *V*2, we define various delays that are shown in Fig. 7.7:

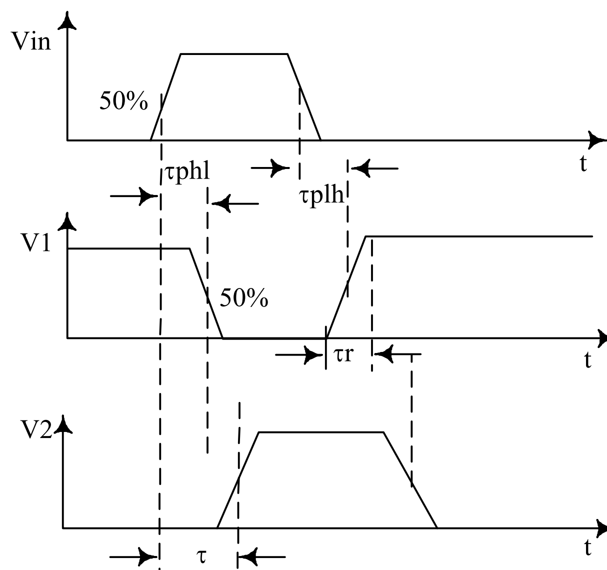


Figure 7.7 Propagation Delays

Copyright © 2000 by John Wiley & Sons

τ_{phl} Propagation delay high to low is the time taken by the output voltage to decrease from V_{OH} to 50% of the logic swing.

τ_{plh} Propagation delay low to high is the time taken by output voltage to increase from V_{OH} to 50% of the logic swing.

τ The propagation delay within one gate is measured from 50% of the logic swing of the input to 50% of the logic swing for the output

The propagation delay within a pair of successive inverters is the sum of τ_{phl} (τ_{plh}) for the driver and τ_{plh} (τ_{phl}) of the load inverter.

τ_f The fall time is the time from the output to fall from 90% to 10% of its high value.

τ_r The rise time is the time for the output to rise from 10% to 90% of its high value.

7.4 Current-Sensing Techniques

Conceptually, current testing is simple, but it requires the following steps after test pattern generation:

1. Apply the test pattern.
2. Wait for the transient to settle.
3. Check the static I_{DDQ} against a certain threshold value.

Current measurement is done externally (off chip) or internally (on chip) to the circuit. The second alternative is preferable with BIST structure. However, measurement of the current is not that simple since the measurement structure may interfere with the measured quantity. A successful current probe should have the following characteristics [Keating 1987]. It must be:

- Easily placed between the CUT and the bypass capacitor at the power supply pin.
- Capable of measuring small static currents.
- Nonintrusive; it does not cause a drop in V_{dd} of more than a few tenths of millivolts.
- Capable of fast measurement, no more than 500 ns per pattern.

Copyright © 2000 by John Wiley & Sons

Switching currents in CMOS circuits are very large and, because of the package pin, inductance may cause a large surge in the voltage at the power and ground rails. For this, a bypass capacitor is needed at the power supply. These large currents tend to mask the small I_{DDQ} and require a long time to settle down the transience.

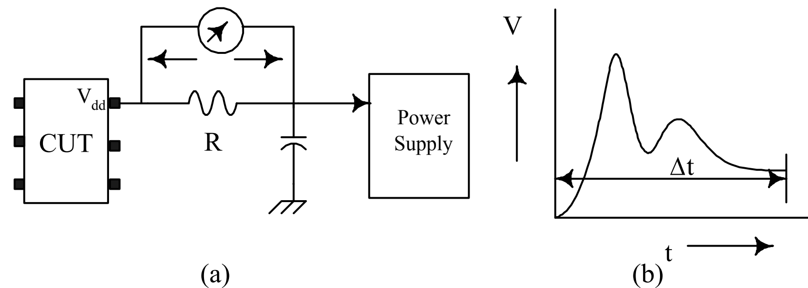


Figure 7.8 Current Measurement (a) Generic Measurement Arrangement, (b) Switching Transient Current

7.4.1 Off-Chip Measurement

A generic representation of current measurement is shown in Fig. 7.8. In this arrangement, a resistance is placed between the V_{dd} pin of the IC and the bypass capacitor of the power supply. The value of this resistance depends on the resolution of the voltmeter and the magnitude of the I_{DD}Q. The voltage drop across the resistance may cause a significant reduction in the voltage at the IC power pin (V_{dd}). Therefore, it is important to build a sensing structure that (1) bypasses the transience and (2) compensates for the voltage drop. Usually, a sense amplifier with sufficient gain is used to measure the quiescent current, as shown in Fig. 7.9a. The op-amp has to be designed such that it compensates for the drop across the probe resistor. It is possible to overcome this voltage drop by shunting the resistor with a diode, but this will cause a drop of 0.6 to 0.8 V. Instead of the diode, a pass transistor can be used. Both shunting methods are shown in Fig. 7.9b. This transistor is on until the transient effect subsides. At such time, the quiescent current will pass through the resistance. To filter the noise at high frequencies, a bypass capacitance, C_{bp}, is used at the output pin of the CUT. This filtering structure will also cause a delay in the stabilization of the circuit for current measurement. However, the testing is not done at speed, and the limiting frequency will depend on the RC_{bp} value.

Copyright © 2000 by John Wiley & Sons

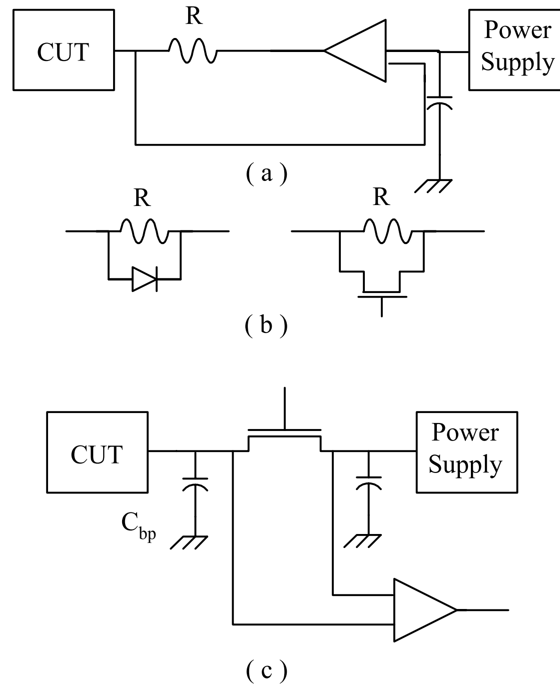


Figure 7.9 Sensing Structures [Keating 1987]:
(a) Use of Op Amp, (b) Bypassing Techniques,
(c) Eliminating the Resistance

A more optimal structure is shown in Fig.7.9c; it is possible to eliminate the resistor and keep the transistor on long enough to bypass the transient current. Afterwards, the quiescent current is strobed. By eliminating the resistance, the circuit becomes faster and more useful over a larger range of currents. While switching transient currents, the transistor offers a short circuit between the two capacitors and maintains full V_{dd} to the CUT. After the transient currents have settled down, the transistor is turned off and the static current is supplied by C_{bp}, as governed by the relation $I = C_{bp} V/ \Delta t$, where Δt is the time necessary for the transience to subside as illustrated in Fig. 7.8b. For a recommended resolution of 25 µA per 10mV, in 500 ns, the by-pass capacitance is then $C_{bp} = I \Delta t/V$ = 1250 pF. To limit the voltage drop across the CUT to 1 V (for V_{dd} = 5V), the current measurement can be done at any time within 50 ms from turning the transistor off. This measurement structure can also be used to measure transient current, I_{DDT}, and has been improved for higher speed probing as described in [Isawa 1997].

7.4.2 On-Chip Measurement

To overcome the limitations of off-chip current probing, on-chip sensors have been proposed [Maly 1988]. They are more commonly known as Built-In Current (BIC) sensors and they have the advantage of increasing the speed and resolution of the measurements. Figure 7.10 shows a basic BIC structure that consists of a voltage-drop device and a

Copyright © 2000 by John Wiley & Sons

voltage comparator. The voltage- drop device is inserted between the ground terminal, V_{GND}, of the device under test and the ground pin of the chip. The voltage V_{GND} is compared to a reference voltage, V_{ref}, which is adjusted such that $V_{GND} < V_{ref}$ for the fault free circuit. When the circuit is defective, then $V_{GND} > V_{ref}$ and this is flagged at the output of the comparator. Several other BIC designs have been proposed [Rius 1992, Miura 1992, Shen 1992, Hurst 1997].

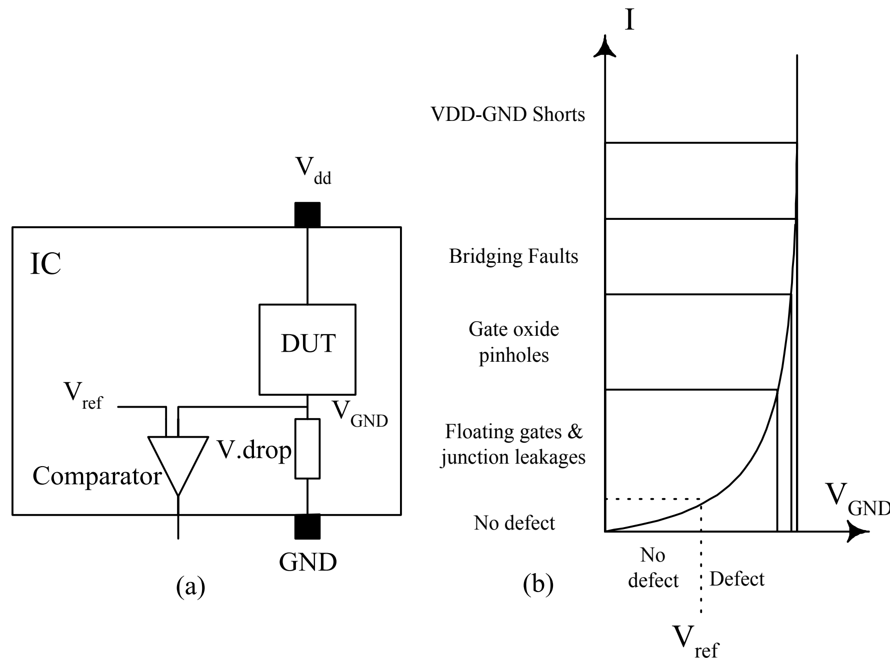


Figure 7.10 On-chip Measurement: (a) On-chip Built-in Current Measurement,
(b) Relation of the Measured Current to the Voltage Drop [Maly 1992]

So far, the voltage-drop device related the current to the corresponding voltage drop as a linear function. However, the magnitude of the faulty I_{DDQ} varies widely with the type of defect as illustrated by Fig. 7.10b. If the voltage drop device measures accurately the small current due to, say, floating gates, the corresponding voltage drop should be large enough to be measurable by the comparator. Therefore, if a linear voltage-drop device is used, it is accurate either with small currents or with large currents, but not with both. A nonlinear element such as a bipolar device is more appropriate for accuracy along a larger range of current [Maly 1992].

7.5 Fault Detection

Consider the NAND implementation of the function *AB* + *C'* that is shown in Fig. 7.11a. Assume that the *p*-channel transistor with input *B* is stuck on. This is equivalent to having the output of the corresponding NAND gate SA1. To provoke the fault from a voltage testing point of view, we must have *AB* = 11. However, to propagate the fault to the

Copyright © 2000 by John Wiley & Sons

output of the circuit (Z), we must, in addition, have $C = 1$. The pattern is, therefore, $ABC = 111$. Next, we examine the effect of the same fault on current flow.

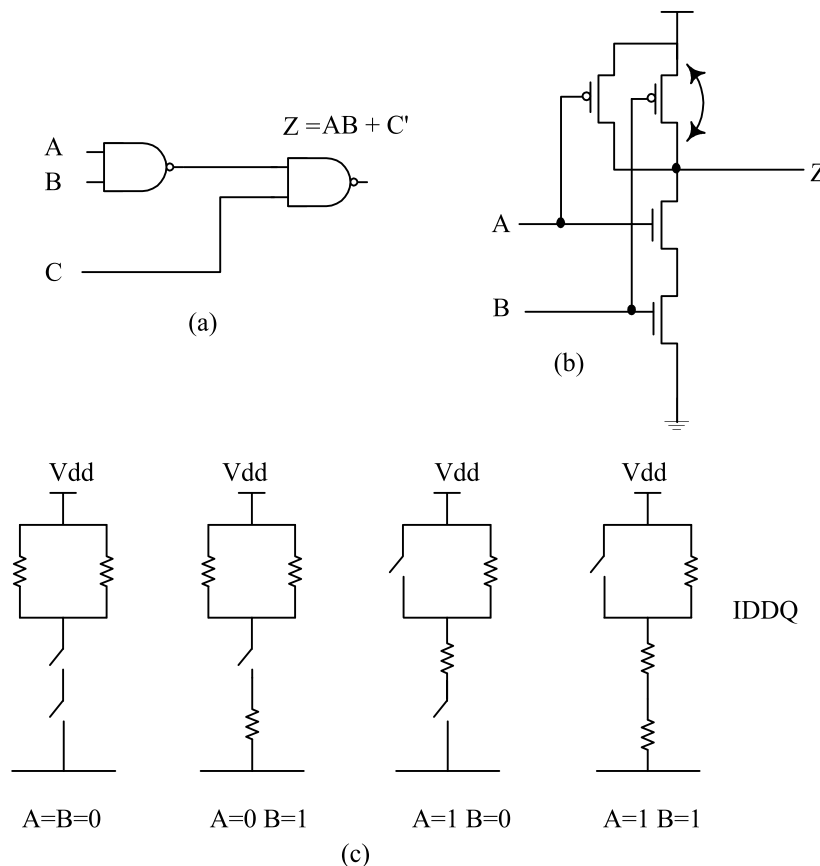


Figure 7.11 Current Testing Fault Detection (a) Circuit Under Test, (b) The NAND Gate with Shorted *p*-channel, (c) States of the Faulty NAND Gate

The behavior of this NAND gate for all possible values of A and B is shown in Fig. 7.11c. For all cases where $A = 0$ or $B = 0$, the circuit is isolated from ground and the output is pulled-up to V_{dd}. Thus the gate appears to behave correctly. For the last case, $AB = 11$, there is a direct path between the V_{dd} rail and ground and the path is active as far as $A = 1$. Therefore, the fault is "directly observable" [Malaiya 1982] and there is no need to sensitize it through the second NAND gate to the primary output of the circuit. Test vectors generated to activate these faults are equivalent to stuck-at fault patterns that guarantee the propagation of the fault to the output of the gate and they are called *pseudo-stuck-at patterns*. In addition to stuck-at and stuck-on faults, I_{DDQ} testing is effective in detecting bridging faults [Acken 1983]and some types of stuck-open faults. Most important, I_{DDQ} uncovers defects that cause leakage current regardless of the fault that models these defects. The concept of a leakage model has been developed and we discuss this first since it encapsulates the underlying principles for other fault detection.

Copyright © 2000 by John Wiley & Sons

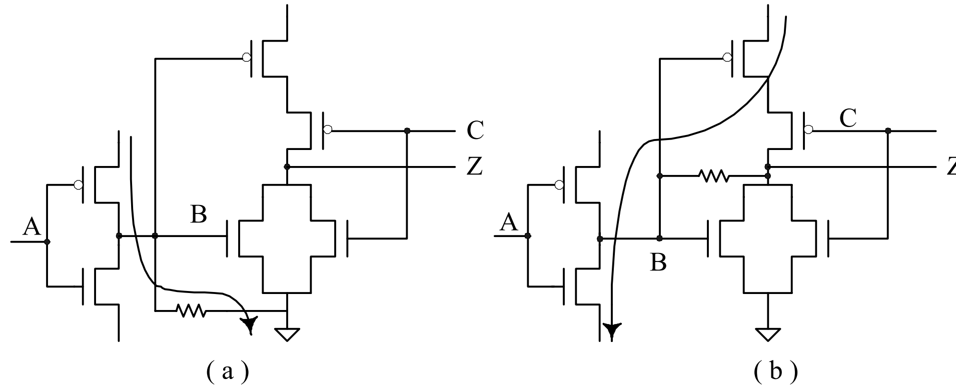


Figure 7.12 Detecting Leakage Faults

7.5.1 Leakage Faults

Defects, which may not affect the logical operation of the circuit, cannot be represented by any of the traditional faults. Some of these defects, such as resistive shorts, may be represented and detected by delay faults. However, it is more likely that testing combines voltage and current testing rather that delay testing. Instead of using delay fault testing, it is more efficient and effective to use current testing and the *leakage fault* model [Mao 1990, Nigh 1990].

In a MOS transistor, current may leak to any other terminal from any of its four terminals – gate (g), source (s), drain (d), and bulk (b). Therefore, there are six leakage faults per MOS transistor in the circuit:

Fgs leakage between gate and source
Fgd leakage between gate and drain
Fds leakage between drain and source
Fbs leakage between bulk and source
Fbd leakage between bulk and drain
Fbg leakage between bulk and gate

Leakage faults between source and drain are SON faults that were used earlier as examples to illustrate the basic concepts of current testing. We consider next other leakage faults such as *Fgs* and *Fgd*. In the NOR gate of Fig. 7.12, a resistive short between *B* and the source of the NMOS transistor cannot be detected within the cell itself since there is no path from V_{dd} through *B* (the gate) and ground (the source). The path has to be traced through the driver of *B* and, more specifically, its PMOS transistor as shown in Fig. 7.12*a*. For this we have $A = 0$, which drives *B* to 1 and the path is formed independently of the other input, *C*. For an *Fgd* of the same transistor, the path is from $V_{dd\ to}$ ground through the PMOS transistors, *C* and *B*, and the NMOS transistor of the driver. This model is used to develop I_{DDQ} test patterns in a subsequent section.

Copyright © 2000 by John Wiley & Sons

7.5.2 Bridging Faults

Bridging faults, discussed first in Chapter 2, are unintentional shorts between nodes in the circuit. The nodes may be 1) the terminals of a transistor (intra-transistor faults), or 2) the terminals of various transistors (inter-transistor faults). It is possible to view the latter as nodes on the logic gate level. On the transistor level, they may be due to gate oxide shorts or punchthrough [Hawkins 1985]. In such cases they can be represented by stuck-at (SAF), stuck-on (SON) faults, and some as stuck-open (SOP) faults. For example, a gate-to-source short, where the source is connected to ground or to V_{dd}, is a SAF, whereas a short between source and drain is a SON fault. A short between gate and source when the source is not connected to ground or V_{dd} acts as a SOP fault. The effectiveness of current testing SAF and SON faults was discussed earlier.

In Chapter 2, we distinguished between those bridging faults that cause an unintended feedback (FB) and those that do not (NFB). A wired-AND or a wired-OR gate generally represents the latter type of faults. Arguably, SSF test pattern can then be used to detect these faults [Millman 1988]. The advantage of using these SSF test patterns is that they are more readily available. Current testing, however, resulted consistently in higher fault coverage in an extensive experiment [Storey 1990]. For a certain circuit, the fault coverage increased from 98.88% to 99.97%. The coverage for SSF patterns is high given that SSFs do not adequately represent many CMOS faults. However, the higher quality of current testing, which is very likely to cost more than SSF testing, would eventually result in a higher defects per million (DPM) that pass the production test. DPM was defined in Chapter 1 [McCluskey 1989]. Using the results plotted in Fig. 1.13, if we use a yield of 90%, the increase in fault coverage by 1% results in a reduction of the DPM from 1000 to 100. Because bridging faults are a predominant problem with CMOS circuits and current testing is very effective in unveiling many defects that are not detectable by voltage testing, efforts have been expanded to generate current testing for bridging faults [Storey 1990], [Ferguson 1991], [Isern 1993], [Bollinger 1994]. FB bridging faults, on the other hand, may cause the faulty circuit to exhibit stable or oscillatory sequential behavior. These faults can be detected by voltage testing using a sequence of two patterns [Xu 1985] and by current testing [Rodriguez 1993], [Roca 1995].

7.5.3 Stuck-Open Faults

Open defects in circuits are the results of errors in manufacturing, as described in Chapter 2. These discontinuities in the interconnections between the terminals of the transistors may cause various effects, depending on the defect location and size. An open defect at the gate of a transistor, as distinguished from the other locations, is usually

Copyright © 2000 by John Wiley & Sons

called a *floating gate*. If the defect is small so that tunneling current can still flow through, the rise and fall times of the signal increase. For a larger open, the input is decoupled from the gate it is supposed to drive. The resulting floating gate acquires a bias voltage that depends on the electrical structure. This voltage can range in any value between 0 and V_{dd} and may turn on the transistor. Thus, depending on the size of the defect and the layout, open faults may or may not be detected.

7.5.4 Delay Faults

In has been concluded from several studies that (a) most CMOS defects cause a timing delay effect rather that catastrophic failures, (b) most of the defects cause elevation of the quiescent current, and (c) any defect that alters the circuit signal path that cause an increase in current will alter the rise and fall times of the signal. This strong correlation between the increase of delays and of quiescent current makes I_{DDQ} testing a viable means to detect delay faults. . When the signal is delayed, it takes longer for the switching current to decay to its quiescent value. It is this differential in timing that helps detect delay faults. It is possible, however, to detect these faults with I_{DDT} testing. With voltage testing, we realized in Chapter 1 that delay faults require a sequence of two vectors for detection. Current testing, however, takes fewer patterns for this detection. A list of some faults and defects uncovered by current testing is shown in Table 7.2 [Soden 1993].

Table 7.2 Relation of defects to SAF and I_{DDQ}.[Soden 1993]

Defect	**SAF**	**I_{DDQ}**
Gate oxide short	Rarely	Yes
Punchthrough (D-S short)	Rarely	Yes
Leaky Junctions	Rarely	Yes
Parasitic leaks	Rarely	Yes
Shorts to rails	Yes	Yes
Open drain or source	No	Sometimes
Open gate with Vin> Vth	Yes	No
Transmission gate	No	Yes
Resistive bridge	No	Yes

Copyright © 2000 by John Wiley & Sons

7.6 Test pattern Generation

Test patterns for current testing are signals to create one or more low-resistance paths from V_{dd} to ground in the presence of defects in CMOS circuits. We describe two approaches. The first uses a switch-level model of the circuit [Rajsuman 1992], and the second uses the leakage fault model given in Section 7.5[Mao 1990].

7.6.1 Switch Level Model-Based

The switch level model uses a connection graph. In this undirected graph, the vertices are the signals V_{dd}, GND, and any intermediate node including the output), and the edges represent the transistors. Each edge is named for the signal controlling the corresponding transistor. The model bears a one-to-one relation to the circuit, and it consists of two sub-graphs, the *p*-graph and the *n*-graph. This is the graph that was used in Chapter 4 for the layout of standard cells. An example of such modeling is shown in Fig. 7.13. A 2-input NAND gate consists of three vertices and two edges for the *n*-graph and two vertices and two edges for the *p*-graph. The combined graphs are shown in Fig.7.13*c*. The dual of this graph represents the two-input NOR gate.

To generate patterns for stuck-on and stuck-open transistors, it is important to trace the path from V_{dd} to GND. For this, all paths from V_{dd} to the output (*p*-graph) or the output to GND (*n*-graph) are identified. Generating test patterns for shorts in the circuit can be summarized as follows: For a short in an *n*-network (*p*-network), a 0 (1) is applied to the faulty edge while 1s (0s) are applied to all other edges. The application of this algorithm to an inverter, a NAND gate and a NOR gate, is shown in Table 7.3.

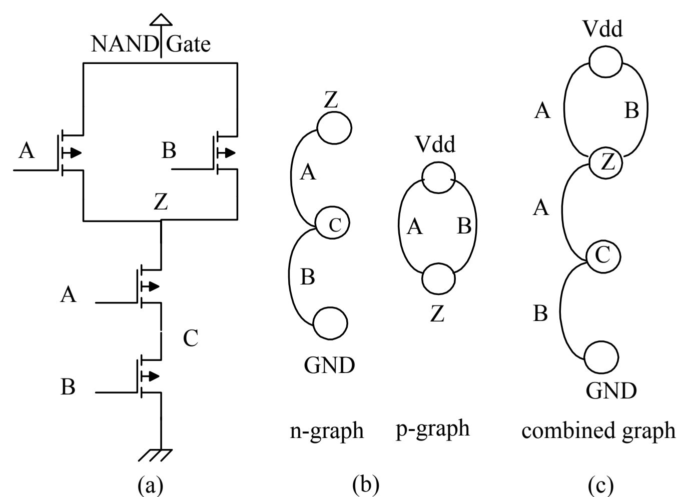


Figure 7.13 Test Pattern Generation for a NAND Gate (a) A NAND Gate, (b) Sub-graphs of the *p*- and *n*-channels, (c) The Combined Graph.

Copyright © 2000 by John Wiley & Sons

Table 7.3. Patterns for Detection of Shorts on the Transistors.

	Inverter		**NAND**		**NOR**	
	Transistor	***A***	**Transistor**	***AB***	**Transistor**	***AB***
***p*-graph**	*A*	1	*A* *B*	11 11	*A* *B*	10 01
***n*-graph**	*A*	0	*A* *B*	01 10	*A* *B*	00 00

We examine next the circuit shown in Fig. 7.14. For each logic gate we can create the patterns in the fashion outlined above. However, it is important next to justify the signal to the primary inputs of the circuit [Rajsuman 1992]. There is, of course, no need to sensitize the output of the gate to a primary output. It be left as an exercise to develop the graphs for the network and generate the patterns. This testing approach is useful for SON and SAF models, but it is not adequate for all possible shorts in the transistors.

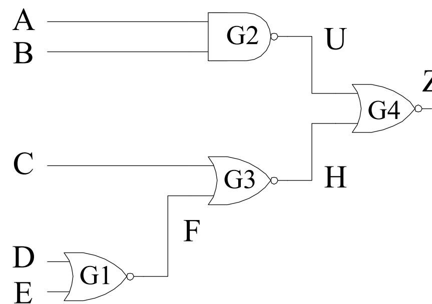


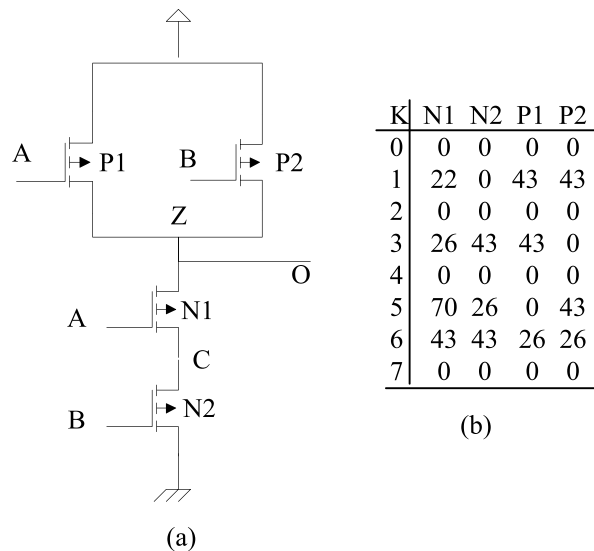
Figure 7.14 Test Pattern Generation, Another Example

7.6.2 Leakage Fault Model-Based

This is a hierarchical test pattern generation approach that utilizes gate-level simulation instead of switch-level simulation. To begin, each cell type is characterized for the detection of all leakage faults within it. This characterization is done only once. The NAND gate shown in Fig. 7.15 is used to illustrate the characterization [Mao 1990]. The results are stored in a table. For each cell with *k* I/O pins, an exhaustive, 2^k test set is used. Each pattern represents a state of the cell. For each pattern, the faults detected on each transistor are entered in the table. Notice that some of these patterns represent illegal cell states. For example, $K = 4$ means that although only one *n*-channel (*A*) is on, the output, *O*, is pulled down. This is not physically possible for a fault-free NAND gate. For similar reasons, patterns 0, 2, and 7 are also illegal. Such patterns are eventually removed from the table. Figure 7.15 shows a NAND gate and its fault table. The first row of the table lists the transistors in the circuit, and *K* is the set (*A, B,*

Copyright © 2000 by John Wiley & Sons

O). The entries in the table are in octal and represent each the 6-tuple {(*Fbg, Fbd, Fbs*), (*Fds, Fgd, Fgs*)}. For example, in the sixth row of the table, the pattern applied is *K*= 5; that is, (*A, B, O*) = (1, 0, 1). For transistor N1, the entry is $(70)_8$ = (111000), indicating that the pattern detected the first three faults of the 6-tuple and did not detect the other three. For transistor N2, the entry is $(26)_8$ = (010110). Therefore, *Fbd, Fds,* and, *Fgd* are detected. No faults were detected for P1 since the corresponding entry in the matrix is 0. The illegal states are removed and the matrix is used as a lookup table in test simulation.



K	N1	N2	P1	P2
0	0	0	0	0
1	22	0	43	43
2	0	0	0	0
3	26	43	43	0
4	0	0	0	0
5	70	26	0	43
6	43	43	26	26
7	0	0	0	0

Figure 7.15 Test Pattern Generation using Leakage Fault Model (a) The Circuit Under Test, (b) The Fault Table

The full circuit is then logic simulated on the gate level using patterns from the functional test vectors. The values of the I/O of all gates are captured. The patterns for current testing are then selected according to the lookup table. The methodology has the advantage of being hierarchical and requiring only logic simulation. Experiments have shown that only 1% of the functional test patterns are needed for current testing. The approach thus streamlines functional testing with current testing.

7.7 Impact of Deep Submicron Technology

Current testing is based on the fact that the quiescent current of the fault-free circuit (defect-free I_{DDQ}) is much smaller than the quiescent current of a defective circuit. However, as indicated in Fig. 7.6, the transistors are still conducting in the off state, $V_{gs} < V_t$. The subthreshold current is a function of the threshold voltage. As the technology feature size decreased, this off-state current increases. Also, the circuits become denser and larger, which

Copyright © 2000 by John Wiley & Sons

contributes to the increase defect-free current. Table 7.4 lists the off-state current per unit length for various feature sizes [Keshavarzi 1997]. The entries for 0.24 and 0.18 are only estimates.

Table 7.4 I_{DDQ} Change with Technology Feature Size [Keshavarzi 1997]

Technolgoy (µm)	V_{dd} (V)	Tox (A)	Vt (V)	Leff (µm)	Ioff (pA/µm)
1.0	5	200	N/a	0.8	4.1E-4
0.8	5	150	0.60	0.55	5.8E-4
0.6	3.3	80	0.58	0.35	0.15
0.35	2.5	60	0.47	0.25	8.9
0.25	1.8	45	0.43	0.15	24
0.18	1.6	30	0.40	0.10	86

As the off-state current is increased, the resolution between the fault-free and defective circuit currents, $M_g - M_d$, of Fig. 7.1 will be reduced. It is even predicted that change of this quantity normalized to M_g will be negligible for CMOS circuit by 2007 [Williams 1996]. Toward improving the discrimination between good and faulty responses, the notion of current signature has been proposed [Gattiker 1998]. This technique does not rely on a single threshold to determine a faulty IC. On the contrary, a *signature* is created by ordering all the measurements by magnitude. The signature is based on the state dependence of the off-state current. Another approach has also been recommended by [Maxwell 1998].

Different physical phenomena contribute to the increase in off-state current [Ferre 1997], [Soden 1996]. For technology features larger than 1 µm, the dominant mechanism is reverse-biased pn junction leakage current. For the submicron technologies, below 0.5 µm, the dominant mechanism is subthreshold leakage current. The decrease in channel length required a reduction in the threshold voltage, V_t, which in turn caused bloating in the subthreshold current as illustrated in Fig. 7.6. The 50% decrease in V_t resulted in current three orders of magnitude higher.

In the past, efforts have concentrated on estimating the current in defective chips [Segura 1992], [Soden 1996]. Nowadays, the concern is becoming more critical to estimate I_{DDQ} for fault-free circuits [Ferre 1997], [Maxwell 1998]. This analysis is needed in order to obtain the upper limit of defect-free I_{DDQ} current to be used as the comparison level for current test (I_{DDQ} Test Limit).

Copyright © 2000 by John Wiley & Sons

To keep current testing effective for future technology, it is important to control the off-state current. Some solutions have been recommended [Williams 1996]:

1. Reverse biasing the substrate during test could give the effect of raising the threshold voltages of the devices and hence reduce the quiescent current [Sachdev 1995], [Keshavarzi 1997], [Liu 1999].

2. Devices could be cooled during testing in order to contain the leakage current. At lower temperatures the threshold voltages can be scaled with the power-supply voltage and without the leakage problem [Gaensslen 1977].

3. Architectural changes such as using dual threshold devices, where possible to minimize I_{DDQ}, could temporarily delay the effect of the calculation in this work. Low V_t devices can be used in parts of the logic where speed is critical, and high V_T devices can be used for other non-critical parts of the design [Taur 1995].

4. The network could be partitioned and I_{DDQ} test performed on individual segments of the design. Individually, selectable footswitch devices with a high V_t value could control the leakage current for the entire network that is implemented with low V_t devices. Power supply buses could be split to reduce leakage current for I_{DDQ} test [Burr 1991].

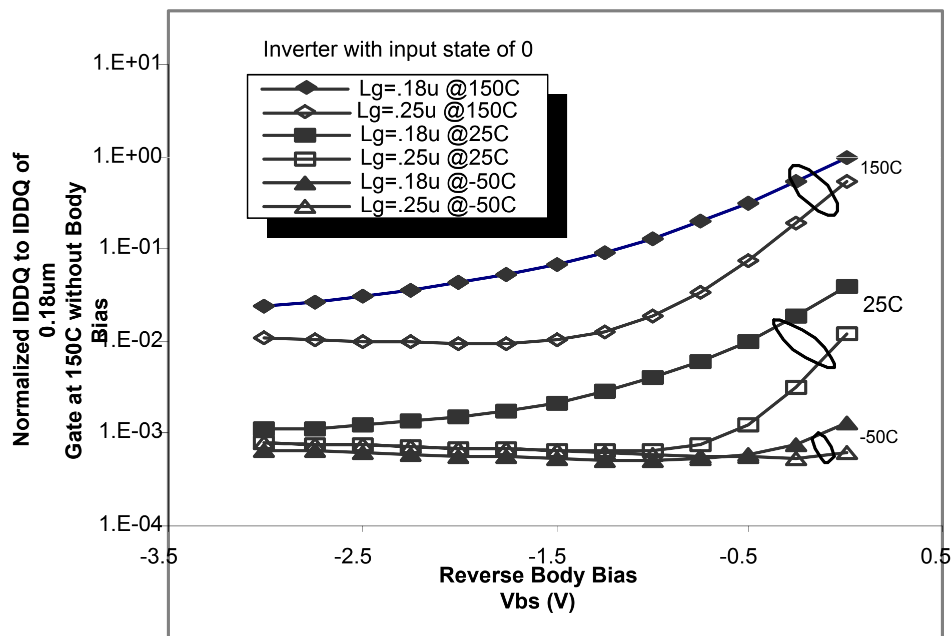


Figure 7.16 Change of the Off-state Current with Back Body Biasing and Temperature {Liu 1999]

Copyright © 2000 by John Wiley & Sons

The effects of the temperature and of reverse body biasing on the off-state current of 0.18-mm deviceshave been investigated in an extensive simulation and measurement study. Some of the results are shown in Fig. 7.16 for a CMOS inverter (input = 0). Two channel lengths are used: 0.18 μm and 0.24 μm. The current is definitely reduced when the temperature is lowered. There is an optimal value of the bias voltage that reduces the off-state current. However, there are no conclusive results on the effectiveness of this approach.

7.8 References

Acken, J., (1983), “Testing for bridging faults (Shorts) in CMOS circuits,” *Proc. Design Automation Conf.*, pp. 717-718.

Bollinger, S.W. and J. Figueras, (1994), “Test Generation for I_{DDQ} Testing of Bridging Faults in CMOS Circuits,” *IEEE Trans. on Computer-Aided Design*, Vol. CAD-13 No. 11, pp. 1413-1418.

Burr, J. and A. Peterson, (1991), “Ultra Low Power CMOS Technology,” *Proc. 3rd NASA Symposium on VLSI Design*, pp. 1-11.

Daniels, R.G., (1990), “The changing demands of microprocessor testing,” *Keynote address, Proc. IEEE Int’l Test Conf.*,.pp. 1-2.

Ferguson, F.J. and T. Larrabee, (1991), “Test Pattern Generation for Realistic Bridge Faults in CMOS ICs,” *Proc. IEEE Int’l Test Conf.*, pp. 492-499.

Ferre, A. and J. Figueras, (1997), “I_{DDQ} Characterization in Submicron CMOS”, *Proc. IEEE Int’l Test Conf.*, p.136.

Fritzemeier, R.R., C.F. Hawkins, and J.M. Soden, (1991), “CMOS IC fault models, physical defect coverage and I_{DDQ} testing,” *Proc. Custom Integ. Circuits Conf.,* pp. 13.1.1-13.1.8.

Gaensslen, F.H. et al., (1977), “Very small MOSFET's for low-temperature operation,” *IEEE Trans. on Electron Devices*, Vol. ED-24 No. 3, pp.218-229.

Gattiker, A.E. and W. Maly, (1998), “Current Signatures: Application,” *Proc. IEEE 1Int’l Test Conf.*, pp. 1168-1177.

Hawkins, C.G. and J.M. Soden, (1985), “Electrical Characteristics and testing considerations for gate oxide shorts in CMOS ICs,” *Proc. IEEE Int’l Test Conf.*, pp. 544-555.

Hawkins, C.F. et al., (1994), “Defect-classes – An overdue Paradigm for CMOS IC Testing.” *Proc. IEEE Int’l Test Conf.,* pp. 413-425.

Hurst , J.P., (1997), “A differential Built-in current sensor design for high-speed I_{DDQ} testing,” IEEE Journal of Solid-State Circuits, Vol. 32, No. 1, pp. 122-125.

Isawa, K. and Y. Hashimoto, (1997), “High-speed measurement circuit,” *Proc. IEEE Int’l Test Conf.*, pp. 111-117.

Isern, E. and J. Figueras, (1993), “Test Generation with High Coverages for Quiescent Test of Bridging Faults in Combinational Circuits,” *Proc. IEEE Int’l Test Conf.*, pp.73-82.

Keating, M., (1987), “A new approach to dynamic IDD testing,” *Proc. IEEE Int’l Test Conf.*, pp. 316-321.

Keshavarzi, A., K. Roy, and C.F. Hawkins, (1997), “Intrinsic Leakage in Low Power Deep Submicron CMOS ICs,” *Proc. IEEE Int’l Test Conf.*, pp. 146-155

Levi, L., (1981), “CMOS is most testable,” *Proc. IEEE Int’l Test Conf.,* pp. 217-220.

Liu, M. and S. Mourad, (1999), “Evaluation of body Biasing Engineering on performance of scaled CMOS devices,” *Proc. SPIE Symposium on Solid State Technology*, pp.

Copyright © 2000 by John Wiley & Sons

Malaiya, Y.K. and S.Y.H. Su, (1982), “A New Fault Model and Testing Techniques for CMOS IC Defects,” *Proc. IEEE Int’l Test Conf.*, pp. 25-34.

Maly, W. and P. Nigh, (1988), “Built-in current testing, a feasibility study,” *Proc. Int’l Conf. On Computer-Aided Design*, pp. 340-343.

Maly, W. and M. Patyra, (1992), “Built-in current testing,” IEEE J. of Solid-State Circuits, Vol. , No. 3, pp. 425-428.

Mao, W. et al., (1990), “Quietest: a quiescent current testing methodology for detecting leakage faults,” *Proc. IEEE Int’l Test Conf.,* pp. 280-283.

Maxwell, P.C. and J.R. Rearick, (1998), “Estimation of Defect-Free I_{DDQ} in Submicron Circuits Using Switch Level Simulation”, *Proc. IEEE Int’l Test Conf.*, p. 882.

McCluskey, E.J. and F. Buelow, (1989), "IC Quality and Test Transparency," *IEEE Trans. on Industrial Electronics,* Vol.36, No. 2, pp. 197-202.

Millman, S.D. and E.J. McCluskey, (1988), Proc. of Int’l Test Conf., pp. 773-783.

Miura, Y. and K. Konishita, (1992), “Circuit design for built-in current testing,” *Proc. IEEE Int’l Test Conf.,* pp. 873-881.

Nelson, G.F. and W.F. Boggs, (1975), “Parametric tests meet the challenge of high-density ICs,” *Electronics*, No. 12l, pp. 108-111.

Nigh, P. and W. Maly, (1990), “Test generation for current testing,” *IEEE Design & Test of Computers*, Vol. 7 No. 2 pp. 26-38.

Noyce, R. N.and M.E. Hoff, Jr., (1991), “A history of microprocessor development at Intel”, *IEEE Micro*, pp. 8-12.

Rajsuman, R. (1992), *Digital Hardware Testing: Transistor-level Fault Modeling and Testing*, Artech House, Norwood, MA

Riezenman, M.J., (1991), “Wanlass’s CMOS Circuit,” *IEEE Spectrum*, Vol. 28 No. 5 , p. 44.

Righter, A.W. et al., (1996), “High resolution I_{DDQ} characterization and testing – practical issues,” *Proc. IEEE Int’l Test Conf.*, pp. 259-268.

Rius, J. and J. Figueras, (1992), “Proportional BIC sensor for current testing,” *Journal of Electronic Testing: Theory and Application*, Vol. 3 No. 4, pp. 387-396.

Roca, M. and A. Rubio, (1995), “Current testability analysis of feedback bridging faults in CMOS circuits,” *IEEE Trans. On CAD.*, Vol. CAD-14 No. 10, pp. 1299-1305.

Rodriguez-Montanes, R., J. Figueras, and A. Rubio, (1993), “Current vs logic testability of bridges in scan chains,” *Proc. European Test Conf.*, pp. 329-396.

Sachdev, M., (1995), “*Iddq* Test and Diagnosis in Deep Sub-micron,” *Proc. IEEE Int’l Test Conf., special session on Iddq*, pp. 84-89.

Segura, J.A. et al., (1992), “Quiescent current Analysis and Experimentation of Defective CMOS Circuits”, *Journal of Electronic Testing: Theory and Applications*, Vol. 3 No. 4, pp. 337-348.

Shen, T. and J.C. Daly, (1992), “On-chip current sensing circuit for CMOS VLSI,” *Proc. IEEE VLSI Test Symposium*, pp.309-314.

Soden, J.M. et al., (1992), “I_{DDQ} Testing: A Review,” *Journal of Electronic Testing: Theory and Applications*, Vol. 3 No. 4, pp. 291-304.

Soden, J. M., R. Gulati,and C. G. Hawkins, (1993), Correct monitoring for efficient detection of CMOS defect and faults, *Tutorial Notes, IEEE Computer Society*, Baltimore, MR.

Soden, J.M., C.F. Hawkins, and A.C. Miller, (1996), “Identifying defects in deep-submicron CMOS ICs”, *IEEE Spectrum*, Vol. 38, No. 9, pp. 66 - 71

Storey, T.M. and W. Maly, (1990), “CMOS Bridging Fault Detection,” *Proc. IEEE Int’l Test Conf.*, pp. 842-850.

Copyright © 2000 by John Wiley & Sons

Taur, Y. et al., (1995), "CMOS scaling into the 21st century: 0.1 μm and beyond," *IBM Journal of Research and Development*, Vol. 39 No. 1/2, pp. 245-260.

Wanlass, F.M. and C.T. Sah, (1961), "Nanowatt logic using field-effect metal-effect metal-oxide Semiconductor triodes," *Proc. Solid State Circuits Conf.*, pp. 32-33.

Williams, T.W. et al., (1996), "I_{DDQ} Test: Sensitivity Analysis of Scaling," *Proc. IEEE Int'l Test Conf.*, pp. 786.

Xu, S. and S.Y.H. Su, (1985), "Detecting I/O and internal feedback bridging faults," *IEEE Trans. on Computers,* Vol. 14 No. 10, pp. 553-557.

7.9 Problems

1. Calculate the peak current for a two-input CMOS NOR gate using minimum feature transistors for 1.2 μm technology and ignore channel length modulation. The transconductance for the *n*- and *p*-channels are 80 and 27 μA/V^2; $L_n = L_p = 1.2$ μm, $W_n = 1.8$ μm, $W_p = 5.4$ μm.

2. For the NOR gate of Problem 7.1, calculate the fall and rise times

3. The I_{DDQ} of a circuit is measured using an external monitor under the following conditions: The transient current has a peak of 2A and lasts for 10ns. The bypass capacitance is 5000 pF and the current is sampled every 200 ns If the voltage across the transistor after it is turned off is 0.8 V estimate the value of the quiescent current. Is the circuit faulty?

4. Using the leakage fault model, develop test patterns for a two-input NOR gate for current testing all intra-transistor bridging faults.

5. Use the switch-level transistor model to determine the patterns to detect the shorts on all the transistors of the circuit in Fig. P7.6.

6. For the transistor level circuit of Fig. 7.P1 estimate the quiescent current of the circuit when $A = 1$, $B = C = 1$, and $A = B = C = 1$.

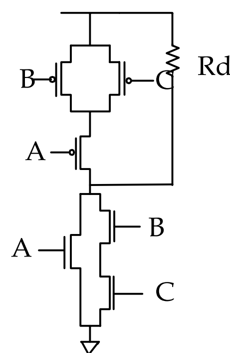


Figure P7.6

Copyright © 2000 by John Wiley & Sons